IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. Specific amendments to individual claims are detailed in the following marked up set of claims.

Please amend the claims as follows:

32. (Amended) A memory circuit, as in Claim 26, wherein the memory circuit is incorporated in an asynchronously-accessible [randon] random access memory.

59. (Once Amended) [An asynchronous dynamic random access] A memory circuit, comprising:
control logic for providing a selected mode control signal;
selection and temporary storage circuitry for receiving and storing a first external address; and
a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode, wherein the memory circuit is an asynchronous dynamic random access memory circuit.

Please add the following new claims:

66. (New) A memory circuit, comprising:
control logic for providing a selected mode control signal;
selection and temporary storage circuitry for receiving and storing a first external address; and
a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit from a pipelined mode to a burst mode.